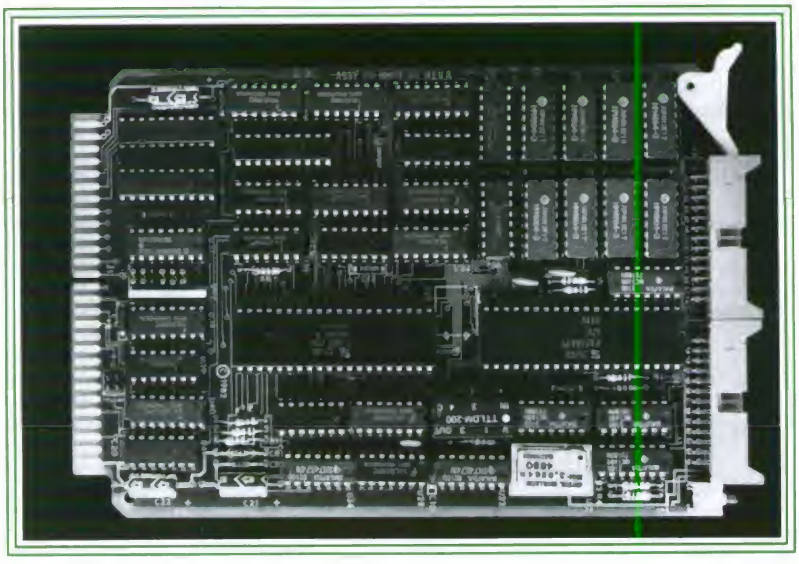
COLEX™

STD-SLAVE

STD BUS



FEATURES

- Fully Buffered Z80A Processor
- STD-Z80 Bus Compatible
- 4 MHz Clock; Independent of Master CPU Speed
- 64K Bytes On-board Dual Ported Ram
- DMA to On-board RAM Supported
- Two Asynchronous RS-232-C Serial Ports
- Supports Interrupt or Polled Operation
- Independent Hardware/Software Reset
- 4 MHz Operation
- Full 1 Year Warranty

DESCRIPTION

The COLEX STD-SLAVE is a powerful multi-function processor board specifically designed to bring multi-processing to the industry standard STD Bus. It features a Z80 microprocessor, two asynchronous serial ports, and 64K bytes of on-board, dual ported, dynamic RAM. In addition, each serial port is driven by an independently programmable baud rate generator. The on-board dual ported RAM may be accessed by either the system Master CPU or the on-board Z80 CPU. This allows communication between the bus and the STD-SLAVE. DMA devices on the bus can also access the STD-SLAVE memory for high speed data transfers.

The concept of multi-processing provides that one or more slave processors are installed on the system bus, are supervised by the bus Master CPU, and operate independently according to instructions stored in on-board memory. The STD-SLAVE board contains all essential elements (CPU, I/O, and memory) of a stand alone microcomputer and is only dependent on the system Master CPU for downloading of programs and communication with shared system resources such as a hard disk.

One application of the STD-SLAVE board is in multi-user CP/M® systems. In this type of system, each user works at a terminal connected to one serial port of a STD-SLAVE board installed on the STD Bus. A serial printer can be connected to the other serial port as well. The operating system and applications programs are downloaded in the STD-SLAVE dual ported RAM from the system master CPU. The STD-SLAVE then operates out of this memory completely independent of any other STD-SLAVE.

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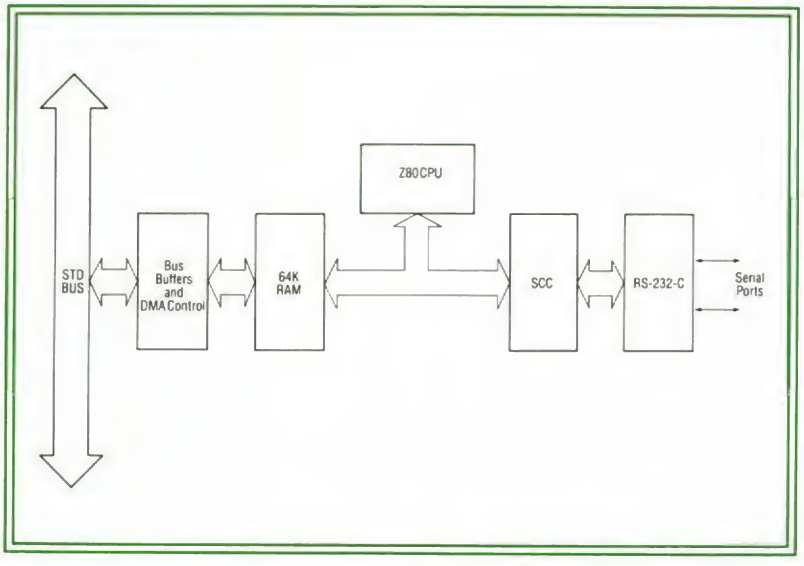
COLEX ASIA PACIFIC Luk Hop Industrial Bldg., 15th Floor, 8 Luk Hop St., San Po Kong, Kowloon, Hong Kong 3/7265651

STD-SLAVE BLOCK DIAGRAM



When the STD-SLAVE requires access to a shared system resource such as a hard disk or special I/O, the system Master CPU directs bus communications. As a result, additional users can be installed on the bus until bus slots and/or power supply capacity is exceeded with no degradation of system performance or response time.

As an intelligent I/O controller, an STD-SLAVE could be used to operate two high speed printers and/or modems. In this application, the STD-SLAVE acts as a printer buffer for printers.

When teamed with a COLEX STD-68000 central processing board running the UNIX™ operating system, the hardware/software Z80 emulator MIMIX™ can be installed to run the industry 8-bit standard operating system CP/M® as a UNIX applications program. This provides access to an enormous number and variety of existing, proven and inexpensive CP/M applications programs and data that can then be operated in the UNIX environment.

SPECIFICATIONS

ELECTRICAL

- System Bus: STD-Z80
- System Clock: 4.0 MHz
- Signal Loading: Inputs: One 74LS load maximum
  Outputs: −3mA min @ 2.4 volts
  24mA min @ 0.5 volts
- On-Board Memory: 64K bytes dual ported RAM
- I/O: 2 serial ports
- I/O Address: Any 4 sequential ports
- Interrupts: Outputs maskable and nonmaskable interrupts to master CPU
- System Interrupt Units: 0 SIUs
- Operating Temperature: 0° to 60° C
- Power Requirements: @ 25° C

Parameter	Condition	Min	Typ	Max	Units
V_{cc}	—	4.75	5.0	4.25	volts
I_{cc}	@ 5V	—	1.05	1.86	A
V_{cc}	—	11.4	12.0	12.6	volts
I_{cc}	@ 12V	—	38	50	mA
V_{cc}	—	−11.4	−12.0	−12.6	volts
I_{cc}	@ −12V	—	36	46	mA

MECHANICAL

- Card Dimensions:

Form Factor	H	W	L	Units
STD Bus	0.60	4.5	6.5	inches

- PC Board Thickness: 0.062 inches
- Connectors:
  STD Bus: 56-pin dual readout; 0.125 inch centers
  Serial: 26-pin dual readout; 0.100 inch grid

ORDERING INFORMATION

Part Number	Description
STD-SLAVE	4 MHz Z80 Based Multi-function SLAVE Processor Board
STM-SLAVE	Technical Manual for STD-SLAVE

MIMIX is a trademark of TouchStone Software, Inc.
CP/M is a registered trademark of Digital Research, Inc.
UNIX is a trademark of Bell Laboratories.

COLEX

STD-SLAVE

* STD-BUS COMPATIBLE
* Z80A-CPU
* 64K BYTES RAM
* TWO RS-232C SERIAL PORTS (DCE)
* SOFTWARE PROGRAMMABLE BAUD RATES 50 TO 19.2K
* OPERATES IN ANY STD-BUS I/O MAPPED ENVIRONMENT
* DUAL PORTED MEMORY ACCESSED BY SLAVE OR MASTER
* 4MHz OPERATION
* 12 MONTH WARRANTY

DESCRIPTION

The COLEX SLAVE brings true multi-processor capability to the STD-Bus. The SLAVE is only dependent on a master CPU to download programs and to provide communication with shared system resources such as discs. Any number of SLAVE CPUs can exist with one master CPU, the number being limited only by the physical size of the backplane and available power. Each SLAVE provides for either polled or interrupt operation and can be reset independently by either hardware or under software control. Application areas for the SLAVE include multi-terminal systems with shared mass storage, intelligent peripheral controllers and communication interfaces.

STD-BUS INTERFACE

The master CPU communicates with the SLAVE CPU via a control word and a status word. There are four control bits in the SLAVE control word. Bit 0 is used to stop the slave processor while the master interrogates the SLAVE memory. Bit1 is used to indicate to the SLAVE processor to restart by use of the SLAVE NMI line. Bit 2 will clear the RESET and SLVFLG flip-flops. Bit 3 issues a reset to the SLAVE processor. Each control bit requires to be pulsed to perform its particular function.

There are three status bits in the SLAVE status word. Bit 0 is the reset flag which indicates that an external reset has been initiated. Bit 1 indicates that the SLAVE internal busses are ready for the master to interrogate the SLAVE memory. Bit 7 indicates to the master that the SLAVE requires service.

Two preloadable address counters are used by the master CPU to determine the location of the SLAVE onboard memory into which it is required to read or write. These counters are loaded in two operations, first the lower byte is written to the MEMORY ADDRESS LOWER register then the upper byte is written to the MEMORY ADDRESS UPPER register. Then by reading or writing to READ MEMORY LOCATION or WRITE MEMORY LOCATION data is transferred to or from the address pointed to by the address counters. Each read to or write from the READ/WRITE MEMORY LOCATION register will increment the address pointer. This allows for ease in transferring blocks of data to or from the SLAVE memory.

The SLAVE Z80A CPU has 64K bytes of on-board dynamic memory. This memory is fully accessible by either the SLAVE or master CPU. A supplemental refresh counter is used to provide a refresh address when the master is controlling the SLAVE.

The SLAVE has two channels of RS-232C serial I/O. In addition each channel has an independently programmable baud rate clock.

SOFTWARE PROGRAMMING

Upon startup the SLAVE operating system is down loaded by the MASTER CPU using the following sequence of steps:

Load the SLAVE address counters pointing to the destination address.

Output data bytes in sequence to the SLAVE memory. This could be performed by a DMA device.

For a system employing more than one SLAVE this operation must be performed for each in turn.

For the SLAVE CPU operating system to request an operation not resident on the SLAVE CPU card, the SLAVE software must set up a buffer readable by the master to indicate the desired external operation. When this has been done the slave executes a halt instruction to indicate to the master that the SLAVE needs service. When the master has completed the transfer operation is restarts the SLAVE by toggling first bit 2 and then bit 1 of the SLAVE control word.

When the MASTER gets a request (interrupt) from a SLAVE the following sequence must take place:

Read each SLAVE's status word

Check for status bit 7 set

If set check for status bit 0 set

If set then reload SLAVE with new operating system otherwise

Send stop command to SLAVE

Load the communication buffer pointer into SLAVE address counter

Read the communication buffer by using an INIR operation

Process request

To output data to the SLAVE the following operation is required:

Load the SLAVE address counter pointing to the destination address

Output data one byte at a time sequentially to the SLAVE

PORT DEFINITIONS

PORT ADDR	READ	WRITE
X0H	STATUS FLAGS	CONTROL WORD
X1H	-	MEMORY ADDRESS LOWER
X2H	-	MEMORY ADDRESS UPPER
X3H	READ MEMORY LOCATION	WRITE MEMORY LOCATION

After a READ or WRITE to memory location at port X3H pointed to by the memory address counter, the counter is incremented to the next address location.

STATUS BIT DEFINITIONS

D0 1 = Push button on SLAVE has been pushed
0 = BUS ACKNOWLEDGED and or any RESET has occurred

D2-D6 Not defined

D7 1 = Slave awaits service

CONTROL WORD BIT DEFINITIONS

D0 1 = STOP OPERATIONS (/BUS REQUEST) (01H)
0 = CONTINUE PROCESSING

D1 1 = RESTART SLAVE OPERATION (/NMI) (02H)
0 = NORMAL

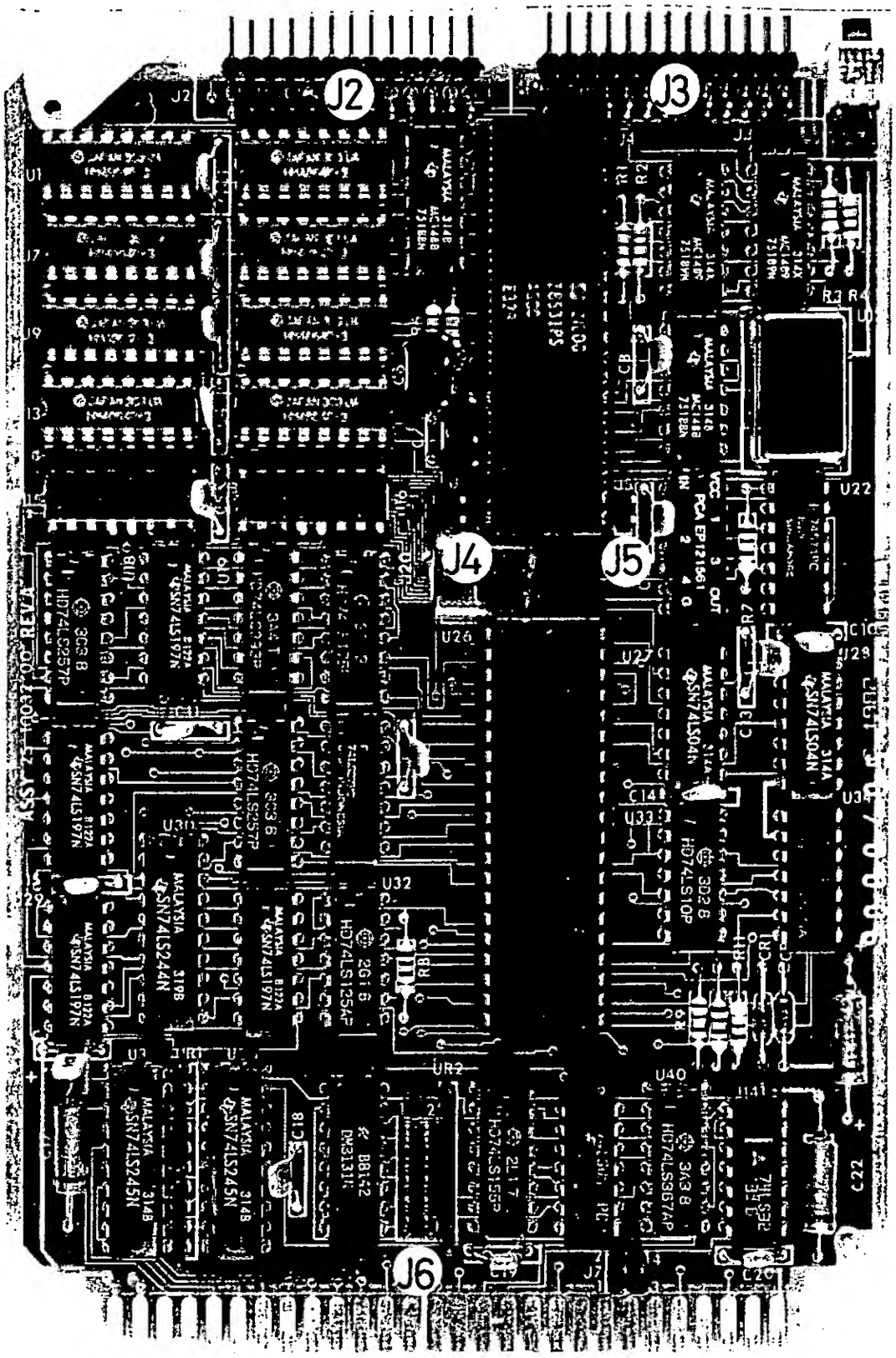
D2 1 = CLEAR SLAVE INTERRUPT FLAG (04H)
0 = NORMAL

D3 0 = RESET SLAVE CMD WORD (07H) (08H)
1 = RELEASE RESET CMD WORD (0FH)

INTERNAL PORT ASSIGNMENTS

PORT ADDRESS	DEVICE
00H	SCC PORT B DATA (terminal)
01H	SCC PORT B CONTROL/STATUS
02H	SCC PORT A DATA (printer)
03H	SCC PORT A CONTROL/STATUS

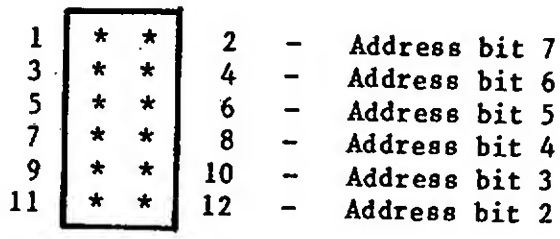
STD-SLAVE HEADER AND CONNECTOR LOCATIONS



PORT ADDRESSING

The jumper header J6 allows the user to select at which I/O port the SLAVE is to be addressed. The following table shows how to determine the strapping for a particular port address.

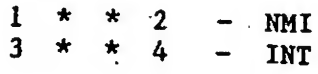
NOTE : open = 1



HEADER J6

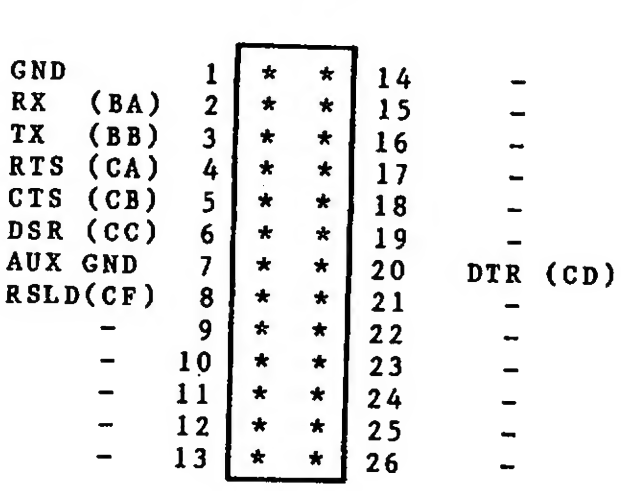
INTERRUPT SELECTION

The jumper header J7 determines whether or not and which of the interrupts will be provided to the master CPU.



HEADER J7

SERIAL I/O CONNECTIONS



TXD	(BA)	Transmit Data
RXD	(BB)	Receive Data
RTS	(CA)	Request to Send
CTS	(CB)	Clear to Send
DSR	(CC)	Data Set Ready
DTR	(CD)	Data Terminal Ready

STD-BUS CONNECTOR

Bus connector: 56 pin dual edge connector, 0.125 inch centers

+5V	1	]	[	2	+5V
GROUND	3	]	[	4	GROUND
nc	5	]	[	6	nc
D3	7	]	[	8	D7
D2	9	]	[	10	D6
D1	11	]	[	12	D5
D0	13	]	[	14	D4
A7	15	]	[	16	A15
A6	17	]	[	18	A14
A5	19	]	[	20	A13
A4	21	]	[	22	A12
A3	23	]	[	24	A11
A2	25	]	[	26	A10
A1	27	]	[	28	A9
A0	29	]	[	30	A8
WR	31	]	[	32	RD
IORQ	33	]	[	34	MEMRQ
IOEXP	35	]	[	36	MEMEX
REFRESH	37	]	[	38	MCSYNC
STATUS1	39	]	[	40	STATUS0
BUSAK	41	]	[	42	BUSRQ
INTAK	43	]	[	44	INTRQ
WAITRQ	45	]	[	46	NMIRQ
SYSRESET	47	]	[	48	PBRESET
CLOCK	49	]	[	50	CNTRL
PCO	51	]	[	52	PCI
AUXGND	53	]	[	54	AUXGND
+12V	55	]	[	56	-12V

ELECTRICAL SPECIFICATIONS

System bus:	STD-Z80
INPUTS	one 74LS load
OUTPUTS	IOH -3mA @ 2.4V
	IOL 24mA @ 0.5V
System clock:	Not used (4MHz internal)
Memory :	64Kb local
Data Bus:	8-bit bidirectional
I/O Address:	4 sequential ports
I/O Capacity:	2 EIA RS-232C serial ports
Baud rates:	50 to 19.2K Baud
Interrupts:	NMI or INT

Operating Temperature: 0 to 60 deg C

Power requirement @ 25 deg C:

1.86 A Max @ 5V dc + 5%
50 mA Max @ 12V dc
46 mA Max @ -12V dc

MECHANICAL SPECIFICATIONS

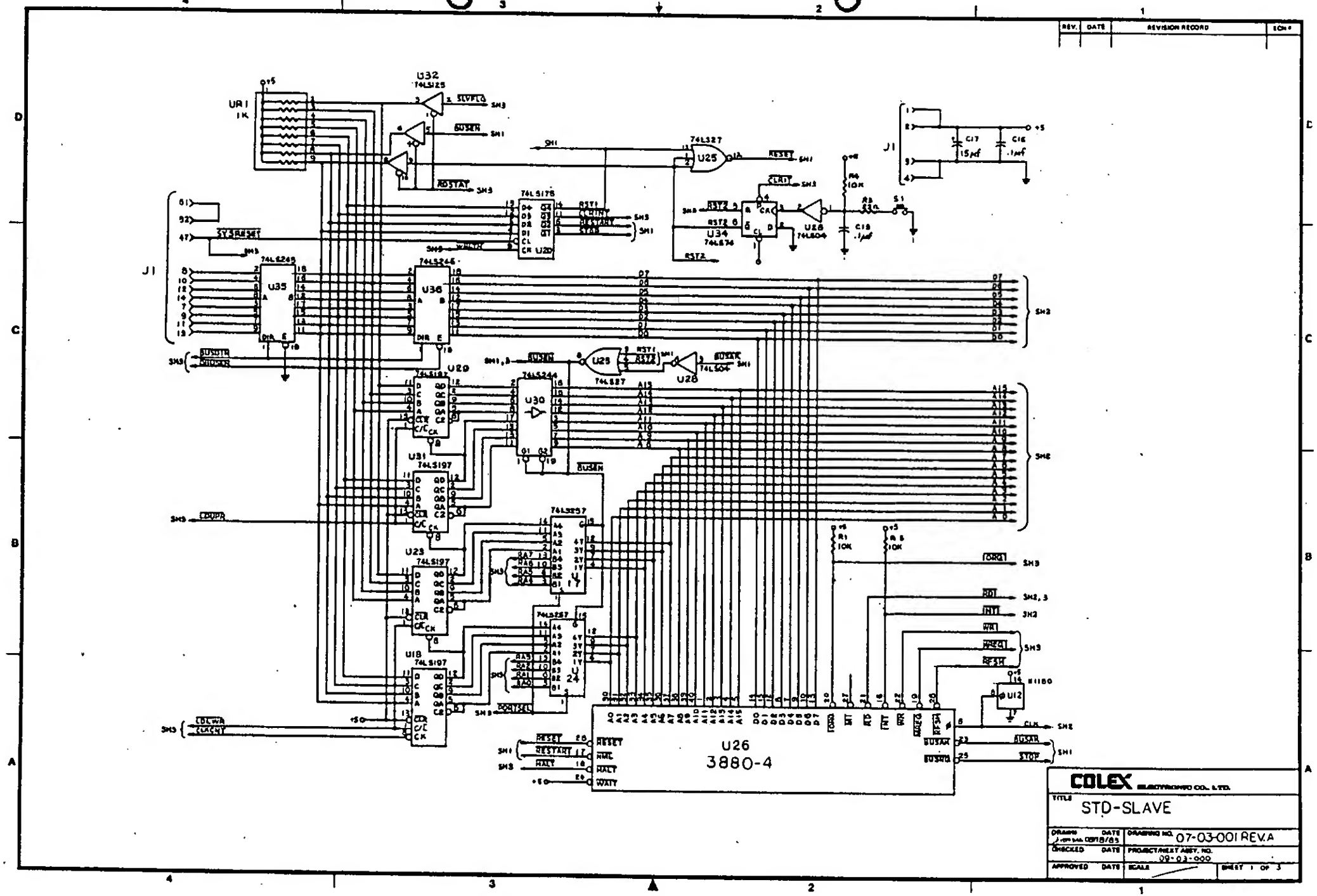
Card dimensions: 0.48 X 4.5 X 6.5 inches
PC Board Thickness: 0.062 inches

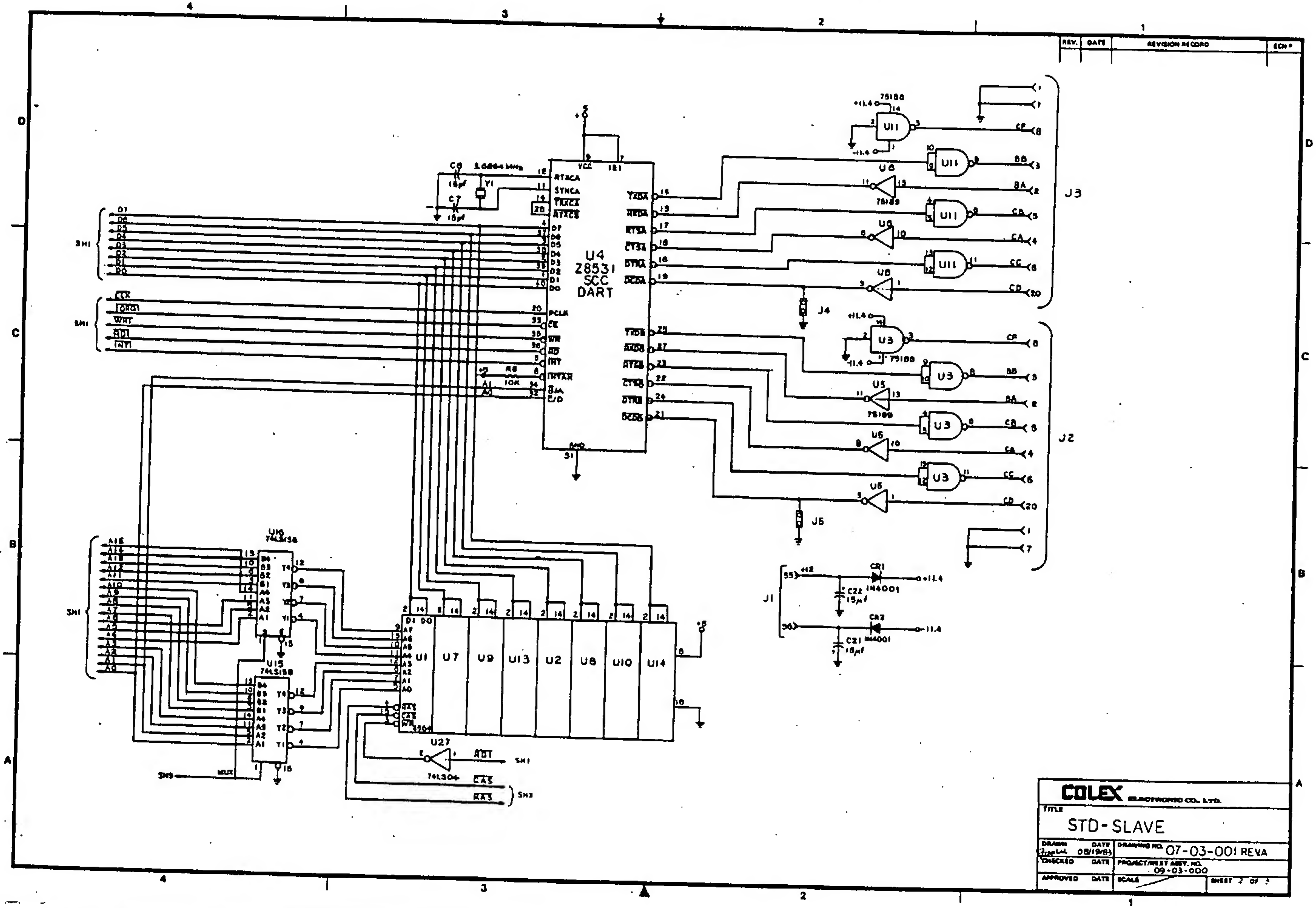
CONNECTORS

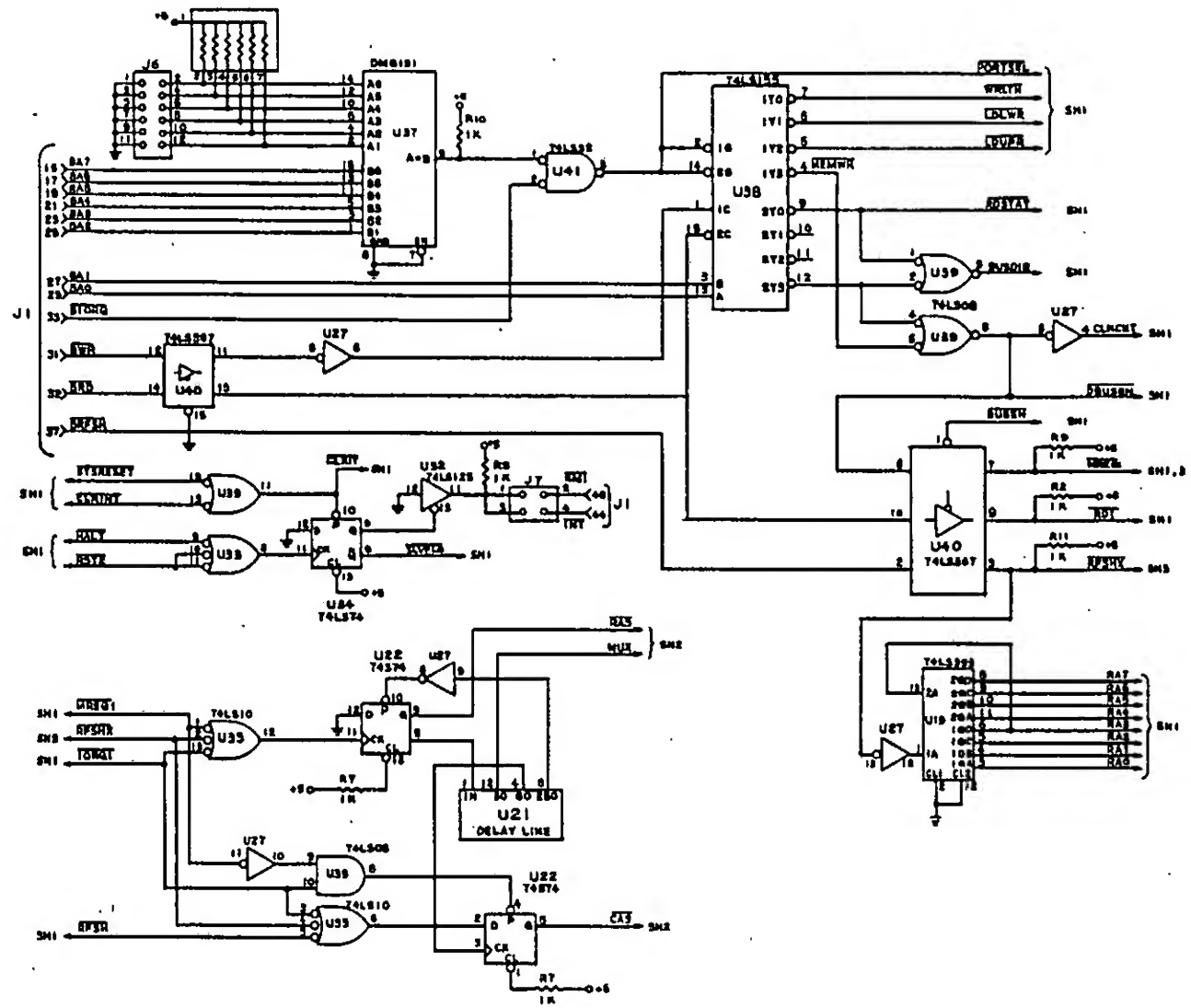
STD-Z80 BUS: 56 pin, 0.125 inch centers

Serial: 26 pin, dual row. 0.100 inch grid

AMERICA	EUROPE	ASIA
COLEX America 15028 Beltway Drive Dallas TEXAS 75234	COLEX (U.K.) Limited Index House Ascot Berkshire	COLEX Electronic Co Ltd 623 Ocean Centre Kowloon Hong Kong
(214) 458-2779	(0990) 23377	3-696194
tlx 703143 colex am	tlx 849426 loninf	tlx 40183 colex hx


REV. | DATE | REVISION RECORD | ECN #
U32
74LS125
UR1
1K
SLVFLG
BUSEN
RDSTAT
74LS175
SYSRESET
74LS245
U35
74LS246
U36
74LS244
U30
74LS27
U25
74LS04
U28
U34
74LS74
J1
C17
15pf
C16
.1mf
C18
.1μf
R4
10K
R5
10K
R1
10K
S1
U29
U31
U23
U18
74LS197
74LS257
U26
3880-4
U12
81LS0
COLWA
CURCNT
DOUTSEL
RESET
RESTART
HALT
WAIT
NMI
BUSAK
BUSRQ
STOP
CLK
COLEX ELECTRONICS CO., LTD.
TITLE
STD-SLAVE
DRAWN
CHECKED
APPROVED
DATE
DRAWING NO. 07-03-001 REV.A
PROJECT/NEXT ASSY. NO. 09-03-000
SCALE
SHEET 1 OF 3


U4
Z8531
SCC
DART
J2
J3
J1
J4
J5
U27
74LS04
U15
74LS158
U16
74LS158
CR1 1N4001
CR2 1N4001
C22 15μf
C21 15μf
3.6864 MHz
COLEX ELECTRONIC CO. LTD.
TITLE
STD-SLAVE
DRAWING NO. 07-03-001 REVA
PROJECT/NEXT ASSY. NO. 09-03-000
SHEET 2 OF 2



REV.	DATE	REVISION RECORD	ECN #

COLEX ELECTRONICS CO., LTD.

TITLE: STD-SLAVE

DRAWN	DATE 88/FEB/8	DRAWING NO.	07-03-001 REV.A
CHECKED	DATE	PROJECT/NEXT ASSY. NO.	09-03-000
APPROVED	DATE	SCALE	SHEET 1 OF 3